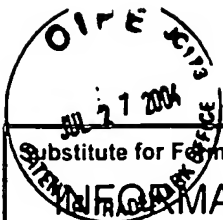


[illegible][illegible]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/810,748
				Filing Date	3/26/04
				First Named Inventor:	Iu-Meng Tom Ho
				Group Art Unit	2824
				Examiner Name	Not yet assigned
Sheet	2	of	2	Attorney Docket Number	02986.P029C

OTHER ART – NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
TT		PCT International Search Report for PCT International Appln No. US02/24267, mailed 10 May 2004 (6 pages).	

Examiner Signature	<i>Imun</i>	Date Considered	5/12/05
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 02986.P029C	Application Number: 10/810,748
	First Named Inventor: Iu-Meng Tom Ho	
	Filing Date:	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (If known)			
TT		6,348,722	Yoshikoshi	02-19-2002	

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
TT		Magma Design Automation, Inc., "Deep-Submicron Signal Integrity", white paper, 2002	
TT		Andrey V. Mezhiba, Eby G. Friedman, "Scaling Trends of On-Chip Power Distribution Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.47-53	
TT		Sani R. Nassif, Onsi Fakhouri, "Technology Trends in Power-Grid-Induced Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.55-59	
TT		Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim, "Analytical Signal Integrity Verification Models for Inductance-Dominant Multi-Coupled VLSI Interconnects", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.61-68	
TT		S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten, "A novel VLSI layout fabric for deep sub-micron applications," in <i>Proceedings of the Design Automation Conference</i> , (New Orleans), June 1999.	
TT		Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Immune VLSI Design using a Network of PLAs Embedded in a Regular Layout Fabric", IEEE/ACM International Conference on Computer Aided Design, ICCAD-2000, November 5-9, 2000, San Jose, CA, USA	
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Examiner Signature	<i>Thien Kue</i>	Date Considered	5/12/05
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